ST10F276-CAA ERRATA SHEET

16-Bit MCU with 832K Byte FLASH and 68K Byte RAM Memories

1 DESCRIPTION

This status sheet describes all the functional and electrical problems known in the CAA silicon version of the ST10F276.

2 FUNCTIONAL PROBLEMS

2.1 PWRDN.1 - Execution of PWRDN Instruction

When instruction PWRDN is executed while pin NMI is at a high level (if PWDCFG bit is cleared in SYSCON register) or while at least one of the port 2 pins used to exit from Power Down mode (if PWDCFG bit is set in SYSCON register) is at the active level, Power Down mode is not entered, and the PWRDN instruction is ignored.

However, under the conditions described below, the PWRDN instruction is not ignored, and no further instructions are fetched from external memory, i.e. the CPU is in a quasi-idle state.

This problem only occurs in the following situations:

a) The instructions following the PWRDN instruction are located in an external memory, and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MTTCx = 0) is used.

Or

b) The instruction preceding the PWRDN instruction **writes** to external memory or an XPeripheral (XRAM, CAN, etc.), and the instructions following the PWRDN instruction are located in external memory. In this case, the problem occurs for any bus configuration.

Note: The on-chip peripherals are still working correctly, in particular the Watchdog Timer, if not disabled, resets the device upon an overflow. Interrupts and PEC transfers, however, cannot be processed. In case NMI is asserted low while the device is in this quasi-idle state, Power Down mode is entered.

No problem occurs if the NMI pin is low (if PWDCFG = 0) or if all P2 pins used to exit from Power Down mode are at inactive level (if PWDCFG = 1): the chip normally enters Power Down mode.

Workaround:

Ensure that no instruction that writes to external memory or to an XPeripheral precedes the PWRDN instruction, otherwise insert a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate wait state is used, the PWRDN instruction must be executed from internal RAM or XRAM.

2.2 XPWM.1 - Consecutive write accesses to the XPWM module

When both following conditions are met:

– code is executed from IFlash

AND

– two (or more) consecutive write operations are executed with XPWM registers as target

Then only the first write operation is performed: the others are not performed.

Workaround:

Add four NOP instructions between two write accesses to XPWM registers.

2.3 XBUS.3 - Corruption of XPWM register on read access

If, fetching from IFlash, a write to XRAM is performed and followed immediately (two MOV instructions in sequence) by a read from a XPWM register, then the XPWM register is corrupted (spurious write) with the content of the data previously written in XRAM.

Workaround:

Insert a NOP instruction before all read accesses to the XPWM module.

2.4 PWRDN.2 - High Current consumption in Power Down mode

When the PWRDN instruction is executed from the Flash (whatever XFlash or IFlash), the Flash is not correctly switched off, leading to a current consumption above the specifications. Moreover, as the XRAM2 and the XFlash are sharing the same XBus chip select, the same behavior occurs when executing the instruction from XRAM2.

Workaround:

Execute the PWRDN instruction from IRAM or XRAM1.

2.5 FLASH.1 - Read while Write not supported

The read while write functionality is not supported with this silicon version: a write operation in one of the four banks prevents subsequent reading from the Flash (whatever XFlash or IFlash) till it is completed.

Workaround:

Flash programming / reprogramming routines must be executed from RAM.

2.6 FLASH.4 - Flash access time

Preliminary characterization data are showing limitations on Flash access time for CPU clock frequency above 40MHz. This can result in erroneous data read from the IFlash or the XFlash for operand accesses or in illegal opcode for opcode accesses.

Workaround:

To have functional parts in the whole -40 / 125 degree Celsius range, limit the CPU clock frequency to 40MHz.

There is no workaround for higher CPU clock frequencies.

2.7 FLASH.6 - P2.0 activity and Flash operations

Activity on pin P2.0 could cause failures during the Flash fetch, read or erase operations. The source of the activity can be external hardware or internal pin activity. This applies when P2.0 is:

– configured in input and connected to a dynamic signal,

– configured in output compare mode or software controlled output.

Workaround:

For fetch and read operations:

– When P2.0 is configured in input, connect it to ground.

– When P2.0 is configured in output:

  –for CPU frequency up to 40MHz, the minimum time between two transitions of the signal must be 90 us;

  –for CPU frequency higher than 40MHz, use P2.0 in static way.

For erase operations: use the pin P2.0 in a static way (input or output).

2.8 RESET.1 - Software and watchdog reset malfunction

The Software reset instruction (SRST) and the Watchdog reset may not be correctly recognized by the Flash controller. As a consequence the Flash controller maintains the ST10 under reset leading to a dead-lock situation.

Workaround:

If the SRST instruction or the watchdog reset are used in the application then the SYSCON register must be configured to activate the bidirectional reset feature and allow the Flash Controller to detect a low level on the $\overline{\text{RSTIN}}$ pin.

Provided that the RPD pin level will remain high for the whole reset duration, the reset will not turn into a hardware reset and the flags in the WDTCON register will be set as before.

To achieve a correct behavior the following constraints must be considered:

1 The circuitry on $\overline{\text{RSTIN}}$ pin must be compatible with the use of the bidirectional reset.

2 $\overline{\text{RSTIN}}$ discharge time must be shorter than the internal Reset duration of 512 CPU clock cycles.

3 RPD pin discharge time must be longer than the time the $\overline{\text{RSTIN}}$ pin is seen at a low level by the ST10F276.

4 $\overline{\text{RSTIN}}$ pulse (low level active) duration must be longer than the PLL Lock Time, in case an unlock occurred.

Application example:

The following values for RC circuitries on the RPD and $\overline{\text{RSTIN}}$ pins have been simulated and are matching the previous constraints.

RPD RC circuit:

R = 215 kohm

C = 100 nF

$\overline{\text{RSTIN}}$ RC circuit:

R = 215 kohm (pull-up to V_{DD})

C = 10 nF (between $\overline{\text{RSTIN}}$ and V_{SS})

Impact on the Alternate Bootstrap Mode:
The Alternate Boot Mode is affected by this functional problem. When the User key is correctly programmed into the Flash, a Software Reset instruction is executed in order to restart the ST10F276 in normal mode and to run the application software.

2.9 PORT.1 - Bit protection not implemented on the CAPCOM IOs of ports P2, P7 and P8

The ST10F276 provides protected bits. These bits can be modified by both the on-chip hardware and the software. This is the case of the Port registers when Alternate functions are in use. The protection ensures that these bits are not modified when the software accesses to other bits of the register.
The Capture Compare Unit (simply CAPCOM) can make a port pin automatically toggling via compare match. If the toggling event occurs during a software modify or write-back operation using any bit manipulation instruction (BSET/CLR, BFLDH/L, BAND,...), performed on another bit of the same port (same data register Px), then the toggling event is overwritten by the write-back.
These bits are the ones related to Port Data registers where the CAPCOM output alternate functions are mapped, see table below.

Table 1. List of the bits affected by the PORT.1 problem

Port Register	Affected Bits	Alternate Function
Port2	P2.0 to P2.15	CC0IO to CC15IO
Port7	P7.4 to P7.7	CC28IO to CC32IO
Port8	P8.0 to P8.7	CC16IO to CC23IO

Workaround 1: Application mapping

Map the application IOs in order not to mix outputs controlled by software on one of those ports when a Compare output is used.

Workaround 2: Software toggling of the Compare output

Instead of using the hardware toggling of the bit, generate an interrupt at each Compare output match. Then inside the interrupt routine a safe port bit manipulation can be performed.

2.10 FLASH.7 - XFlash access and wait-state

Preliminary characterization data are showing limitations on XFlash access time for CPU clock frequency above 33MHz with 0 wait-state (see register XFICR programming).

Workaround:
For CPU frequencies above 33MHz, configure XFICR to have 1 wait-state.

Note that the default value of the XFICR after reset is such that 15 wait-states are used to access the XFlash.

2.11 XSSC.1 - XSSC Receive Error Flag not set

In the following conditions:

– 2 data (Data_A and Data_B) are consecutively received on the XSSC

– the XSSC Receive Buffer (XSSCRB) is read (by the CPU) at the end of the reception of the second data

Then the XSSCRB register content is updated with Data_B by the XSSC module. The Data_A is lost and the Receive Error Flag is not set in the XSSCCON register. As the reception of the Data_B sets the XSSC Receive Interrupt Flag, the CPU will read Data_B as the second data received.

Therefore Data_B will be read twice with no error flag.

Additional information:

The item is valid in both master and slave modes.

This is impacting the application when transmissions are made consecutively without stopping the clock as described below.

To initiate the clock, a dummy transmission is made by the master: i.e. the application code writes to the XSSCTB (transmit buffer) and a clock is generated, data is received along with this clock.

When several data are to be received, generally the application uses the XSSC Transmit Interrupt Request flag. As soon as the XSSCTB has been transferred to the shift register, the XSSC Transmit Interrupt Request flag is set to indicate that the XSSCTB can be reloaded again. This gives the fastest transmission as a continuous clock is provided to the slave. The application checks the XSSC Receive Interrupt Request flag to read the received value and a new reception is on going during the effective reading of XSSCRB register.

Workaround:

When the ST10F276's XSSC is in master mode, do not use continuous transfer sequences. Instead wait for the complete reception of each data, using the XSSC Receive Interrupt Request flag before starting a new reception.

When the ST10F276's XSSC is in slave mode (or in master mode), the real time behavior of the application must be checked. The polling rate of the XSSC Receive Interrupt Request flag or the priority of the XSSC Interrupt must be increased in order to ensure the reading of the XSSCRB before the end of the next transfer.

2.12 XASC.1 - XASC Receive Overrun Error Flag not set

In the ST10F276's XASC, data reception is double buffered, so that reception of a second character may begin before the previously received data has been read out of the receive buffer register (XS1RBUF). The overrun error flag (S1OE, bit 10 of XS1CON register) and an error interrupt request flag will be set when the receive buffer has not been read out before the completion of the second reception.

In the condition where the XS1RBUF register content is read out at the completion of the second reception, the XS1RBUF register content is updated and the new data is read out without the flags being set.

Workaround:

The real time behavior of the application must be checked. The polling rate of the XASC Receive Interrupt Request flag or the priority of the XASC Receive Interrupt must be increased in order to ensure the reading of the XS1RBUF before the end of the next transfer.

3 FUNCTIONAL PROBLEMS SUMMARY

Table 2. Functional Problems' List

Functional Problem	Short Description
FLASH.1	Read While Write not supported
FLASH.4	Flash access time
FLASH.6	P2.0 activity and Flash operations
FLASH.7	XFlash access and wait-state
PORT.1	Bit protection not implemented on ports P2, P7 and P8
PWRDN.1	Execution of PWRDN Instruction
PWRDN.2	High current consumption in Power Down Mode
RESET.1	Software and Watchdog reset malfunction
XBUS.3	Corruption of XPWM register on read access
XPWM.1	Consecutive write accesses to the XPWM module not performed
XSSC.1	XSSC Receive Error Flag not set
XASC.1	XASC Receive Overrun Error Flag not set

4 DEVIATIONS FROM DC/AC SPECIFICATION

4.1 DC Parameters

Engineering data are under collection.

4.2 AC Parameters

Engineering data are under collection.
One limitation have been found:
T_{LOCK}: PLL Lock-in time for x10 multiplication factor is 300us instead of 250us.

5 DOCUMENTATION UPDATE - MODIFICATIONS OF FEATURES

Previous reference: ST10F276 Design Advance Data, Edition 2.0, 8 Feb. 2003
New reference: ST10F276 Preliminary Data, Revision 1.0, March 2004

5.1 Flash commands timings updated

Characterization and validation results were showing that the typical programming and erasing times for the Flash are longer than the original specified values. This point was formerly described as FLASH.3 functional problem.

Specification change:
Timings for erase and programing are now fully specified.

5.2 Main Voltage regulator must be OFF in Power Down

Characterization and validation results show that the main voltage regulator must be switched off during Power Down to meet power consumption specification and avoid possible CPU wake-up. This point was formerly described as PWRDN.3 functional problem.

Specification change:
The main voltage regulator must be turned off in Power Down by setting bit VREGOFF in XMISC register (bit XMISC.3). Setting this bit will automatically turn-off the main voltage regulator after the Power Down instruction is executed and will turn it up again when leaving Power Down mode.

5.3 DC and AC parameters modifications

The following parameters were formerly highlighted as out of the target specifications. They have now been re-specified in the “Preliminary Data”, edition 1.0.

V_{HYS} (Input Hysteresis in TTL threshold): this parameter is re-specified to 400mV instead of 500mV.

I_{SB1} (Stand-by mode current with RTC off, Oscillator off and V_{DD} off): for temperature within 105 / 125 degree Celsius this parameter is re-specified to 500uA instead of 200uA.

VCO frequency range: the VCO frequency range have been re-specified to 64-128MHz instead of 40-128MHz.

I_{OV2} (Overload current on pin P2.0): This is a new parameter. The overload currents for the pin P2.0 are restricted to +5 / -1 mA instead of +5 / -5 mA for the other input pins.

6 ERRATA SHEET VERSION INFORMATION

This document reflects the current silicon status of the ST10F276-CAA. The major revision of the device can be read in the IDCHIP register (@F07Ch) which is set to 1143h for the ST10F276-CAA version.

Table 3. Revision History

Date	Revision	Description of Changes
March 2004	1	First Issue.
September 2004	2	Added FLASH.7 and I_{OV2} items. Modified FLASH.1 and FLASH.6 items. Added AC deviation on parameter T_{LOCK} in section Deviations from DC/AC specifications. Applied latest “Document Format Standards”.
September 2004	3	Added XSSC.1 and XASC.1 items.

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